UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
CZEKAJ, DAVID J

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/052,552	PARK ET AL.
	Examiner	Art Unit	
	Dave Czekaj	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 July 2005</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-25</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-25</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments with respect to claims 1-25 have been considered but are

moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ozkan et al. (5933451), (hereinafter referred to as "Ozkan") in view of Kato (6271774).

Regarding claim 1, Ozkan discloses an apparatus that relates to

determining the complexity of a data signal (Ozkan: column 1, lines 3-5). This

apparatus comprises "a channel data processor comprising a frame buffer group

including a plurality of frame buffers for each input channel, the channel data

processor for selecting data transmitted to the frame buffer group to output the

selected data, wherein the channel data processor stores each unit of the frame

data into the buffer group" (Ozkan: figures 1-3, wherein the channel data

processors are the processors, the frame buffer group are each of the frame

buffers of each processor, the selection is performed by the multiplexer) and "an

encoder for encoding image signals output from the processor with a MPEG

method" (Ozkan: figures 2-3, wherein the encoder is the MPEG encoder).

However, Ozkan fails to disclose the set-up input channel selection order as claimed. Kato teaches that prior art computing systems introduce long delay times when performing multiple calculations (Kato: column 6, lines 51-55). To help reduce this delay time, Kato discloses using a "set-up input channel selection order" (Kato: column 9, lines 1-15, wherein the set-up channel selection order is control signal). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to take the apparatus disclosed by Ozkan and add the selection order taught by Kato in order to obtain an apparatus that operates more efficiently by reducing the processing delay time.

Regarding claim 2, Ozkan discloses "outputting the frame data stored in the buffer group to the encoder" (Ozkan: column 4, lines 66-67 – column 5, lines 1-7).

1.   Claims 3-14, 18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozkan et al. (5933451), (hereinafter referred to as "Ozkan") in view of Kato (6271774) in further view of Honda et al. (6493466), (hereinafter referred to as "Honda").

Regarding claims 3, 10, and 18, note the examiner's rejection for claim 1, and in addition, claims 3, 10, and 18 differ from claim 1 in that claims 3, 10, and 18 further require two switches to connect the input channels, buffers, and output to encoders. Honda teaches that switches contacting the input channels with a buffer and switches contacting the frame buffer for outputting data to the encoder

can precisely control an encoder (Honda: figure 5, wherein the first switch unit is

switch 102, the second switch unit is switch 108/104, column 9, lines 22-47,

wherein the precise control is the use of the switches to supply the data to the

necessary locations). Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to take the apparatus

disclosed by Ozkan, add the selection order taught by Kato and add the

switching units taught by Honda in order to obtain an apparatus that more

precisely controls the compression of data.

Regarding claim 4, Honda discloses "the first switch unit stores each unit

of frame data in accordance with a set-up channel selection order, the second

switch unit contacting with the frame buffer group in accordance with a set-up

channel contact order and outputting the frame data"(Honda: column 9, lines 22-

47, wherein the selection order is alternatively inputting the pictures between the

two buffers).

Regarding claim 5, Honda discloses "a discrete cosine transformer"

(Honda: figure 17, item 1703), "a quantizer" (Honda: figure 17, item 1704), "an

inverse quantizer" (Honda: figure 17, item 1708), "an inverse discrete cosine

transformer" (Honda: figure 17, item 1709), "a prediction memory" (Honda:

figure 17, item 1711), "an adder" (Honda: figure 17, item 1710), and "a

subtracter" (Honda: figure 17, item 1702).

Regarding claims 6 and 12, Honda discloses "a variable length encoder

and outputting the encoded signals" (Honda: figure 17, item 1705) and "a parser

for loading channel information about each frame and outputting the signals"

(Honda: figure 17, column 17, lines 60-65, wherein the parser is the synthesizing

unit, the information about each frame is the information indicating that the image

has not been skipped).

Regarding claim 7, Kato discloses "a channel selection unit including a

key for setting up a select pattern in regard to the input channels" (Kato: column

9, lines 1-15, wherein the key for setting up a select pattern is the control signal)

and "a channel controller for controlling the first and second switch unit in

accordance with the select pattern" (Kato: column 9, lines 10-17).

Regarding claim 8, note the examiner's rejection for claims 1, 2, and 4.

Regarding claim 9, note the examiner's rejection for claim 1 and in

addition Honda discloses "encoding signals by using previous frame data stored

in the prediction memory" (Honda: column 9, lines 44-52, wherein the

compression encoder performs the encoding, the previous frame data is the

second image).

Regarding claim 11, note the examiner's rejection for claim 5 and in

addition Honda discloses "a prediction memory selection unit for controlling

prediction memory of channels corresponding to the selected channels by the

second switch unit to be contracted between the adder and subtracter" (Honda:

figure 17, wherein the controlling is performed by the motion amount detector).

Regarding claims 13 and 22, note the examiner's rejection for claim 7 and

in addition Honda discloses "a channel controller for controlling the prediction

memory" (Honda: figure 17, wherein the controlling is performed by the motion

amount detector).

Regarding claim 14, note the examiner's rejection for claim 9 and in

addition Honda discloses "selecting a prediction memory of channels

corresponding to the input frame with numbers corresponding to the number of

input channels" (Honda: figure 17, wherein the switch 1717 selects whether to

engage the prediction memory or image memory).

2.   Claims 15-17, 19, 20-21, and 23-25 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Ozkan et al. (5933451), (hereinafter referred to as "Ozkan") in view of

Kato (6271774) in further view of Honda et al. (6493466), (hereinafter referred to as

"Honda") in further view of Faryar et al. (6625215), (hereinafter referred to as "Faryar").

Regarding claim 15, note the examiner's rejection for claims 1 and 3, and

in addition claim 15 differs from claims 1 and 3 in that claim 15 further requires

calculating a similarity between images. Faryar teaches that prior art

compression systems require a great overhead to be sent to the decoder (Faryar:

column 1, lines 54-60. To help alleviate this problem, Faryar discloses "an

encoder for calculating a similarity by comparing image signals output from

processor and previous frame data and selecting one mode set up differently for

each other in regard to the present frame data in accordance with the calculated

similarity" (figure 7, wherein the similarity is calculated from the comparison,

column 6, lines 31-35, wherein the mode is the intra/inter mode). Therefore, it

would have been obvious to one having ordinary skill in the art at the time the

invention was made to take the apparatus disclosed by Ozkan, add the selection order taught by Kato, add the switching units taught by Honda, and add the similarity computing means taught by Faryar in order to obtain an apparatus that operates more efficiently by reducing computational overhead.

Regarding claim 16, discloses "a first mode for encoding the present frame data with an intra coding method" (Faryar: column 6, lines 31-35, wherein the first mode is the intra mode) and a "second mode for encoding data by subtracting the previous frame data from the present frame data" (Faryar: column 6, lines 31-31, wherein the second mode is the inter mode).

Regarding claim 17, note the examiner's rejection for claim 15 and in addition Faryar discloses "outputting encoding mode information" (Faryar: column 6, lines 55-57, wherein the mode information is sent or output to the encoder and decoder).

Regarding claim 19, Faryar discloses "an intra frame coder" (Faryar: figure 3, item 114), "and intra frame decoder" (Faryar: figure 3, item 116), "an adder" (Faryar: figure 3, item 132), "a subtracter" (Faryar: figure 3, item 126), and "a frame memory selection unit for controlling the frame memory of channels" (Faryar: figure 3, items 112, 112A, 112B, 118, wherein the frame memory selection unit is the coding mode selector which controls the switches which controls the frame memory).

Regarding claims 20 and 25, Faryar discloses "a similarity calculation unit calculating a similarity by comparing previous screen data and frame data of

selected channel and determining an encoding mode with the macro block unit"

(Faryar: figure 3, column 5, lines 46-50, wherein the previous screen data is the

previously constructed sample, the mode is the inter/intra mode).

Regarding claims 21 and 23, Faryar discloses "determining a calculated

similarity as the first mode when the calculated similarity is greater than a set-up

reference value, and as the second mode when the calculated similarity is less

than a set-up reference value" (Faryar: column 6, lines 31-35, wherein the set-up

reference value is the inter/intra threshold, the two modes are the intra mode and

the inter mode).

Regarding claim 24, note the examiner's rejections for claims 16 and 21.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dave Czekaj whose telephone number is (571) 272-

7327. The examiner can normally be reached on Monday - Friday 9 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mehrdad Dastouri can be reached on (571) 272-7418. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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PRIMARY EXAMINER